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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

#8/Amdt A
R. Tyson
9/19/01

IN RE APPLICATION OF: :

YASUAKI SEKI ET AL : EXAMINER: PATEL

SERIAL NO.: 09/539,864 :

FILED: MARCH 31, 2000 : GROUP ART UNIT: 2841

FOR: INSULATING RESIN COMPOSITION FOR MULTILAYER PRINTED-WIRING BOARD

AMENDMENT AND REQUEST FOR RECONSIDERATION

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

9/19/01

Responsive to the Official Action dated April 11, 2001, Applicants respectfully request reconsideration of the above-identified application in view of the following amendments and remarks.

IN THE SPECIFICATION

Page 5, please rewrite the paragraph at lines 16-23, as follows:

A'

Further, with the line width and the width between the lines being reduced, filler 4 having a still smaller particle diameter is demanded; however, the filler 4 can only be reduced in particle diameter to about 10 μm at the smallest, and if one or five minutes of processing is performed in such a state, a problem also arises that the bonding strength between the insulating layer and the conductor layer is lowered.

IN THE CLAIMS

Please cancel Claims 1 and 2, without prejudice toward the further prosecution of these claims in a Continuation and/or Divisional Application.

Please add the following new claims:

3. (New) A method for forming unevenness on the surface of an insulating layer, comprising:

(1) plasma etching a layer of an insulating resin composition, to obtain a plasma-treated insulating layer,

wherein said resin composition comprises a first resin and a second resin, and said first resin and said second resin have different plasma etching rates and said first resin and said second resin are not compatible with each other.

4. (New) The method of Claim 3, wherein said plasma-treated insulating layer has a surface roughness of 100 nm to 4,000 nm.

5. (New) The method of Claim 3, wherein said insulating layer comprises a resin selected from the group consisting of polyamide resins; epoxy resins; cyanate ester resins; polyether sulfone resins; polyphenylene ether resins; diallyl phthalate resins; polyurethane resins; polyester resins; phenolic resins; phenoxy resins; resins obtained by polymerizing two or more monomers selected from the group consisting of butadiene, acrylonitirle, styrene, and (meth)acrylate; and mixtures thereof.

6. (New) The method of Claim 3, wherein said insulating layer comprises an epoxy resin and a polyamide resin.

7. (New) The method of Claim 6, wherein said polyamide resin has a plasma etching rate which is higher than the plasma etching rate of said epoxy resin.

8. (New) The method of Claim 3, wherein said insulating layer is formed on a

surface of a substrate and said substrate comprises a wiring pattern on said surface of said substrate.

9. (New) The method of Claim 8, further comprising forming holes in said insulating layer to expose a portion of said wiring pattern.

10. (New) The method of Claim 3, wherein said plasma etching is reactive ion etching and with argon gas as an etching gas.

11. (New) A method for producing a multilayer printed-wiring board, comprising:

(1) plasma etching a layer of an insulating resin composition, to obtain a plasma-treated insulating layer; and

(2) forming a conducting layer on said plasma-treated insulating layer,

wherein said resin composition comprises a first resin and a second resin, and said first resin and said second resin have different plasma etching rates and said first resin and said second resin are not compatible with each other.

A2 cont.

12. (New) The method of Claim 11, wherein said plasma-treated insulating layer has a surface roughness of 100 nm to 4,000 nm.

13. (New) The method of Claim 11, wherein said insulating layer comprises a resin selected from the group consisting of polyamide resins; epoxy resins; cyanate ester resins; polyether sulfone resins; polyphenylene ether resins; diallyl phthalate resins; polyurethane resins; polyester resins; phenolic resins; phenoxy resins; resins obtained by polymerizing two or more monomers selected from the group consisting of butadiene, acrylonitirle, styrene, and (meth)acrylate; and mixtures thereof.

14. (New) The method of Claim 11, wherein said insulating layer comprises an epoxy resin and a polyamide resin.

15. (New) The method of Claim 14, wherein said polyamide resin has a plasma

etching rate which is higher than the plasma etching rate of said epoxy resin.

16. (New) The method of Claim 11, wherein said plasma etching is reactive ion etching and with argon gas as an etching gas.

17. (New) The method of Claim 11, wherein said insulating layer is formed on a surface of a substrate and said substrate comprises a wiring pattern on said surface of said substrate.

18. (New) The method of Claim 17, further comprising forming holes in said insulating layer to expose a portion of said wiring pattern.

A2 Cont'd

19. (New) A multilayer printed-wiring board, which is prepared by a process comprising:

(1) plasma etching a layer of an insulating resin composition, to obtain a plasma-treated insulating layer; and

(2) forming a conducting layer on said plasma-treated insulating layer,

wherein said resin composition comprises a first resin and a second resin, and said first resin and said second resin have different plasma etching rates and said first resin and said second resin are not compatible with each other.

Sub B1

20. (New) The method of Claim 19, wherein said plasma-treated insulating layer has a surface roughness of 100 nm to 4,000 nm.

21. (New) The multilayer printed-wiring board of Claim 19, wherein said insulating layer comprises an epoxy resin and a polyamide resin.

22. (New) The multilayer printed-wiring board of Claim 20, wherein said polyamide resin has a plasma etching rate which is higher than the plasma etching rate of said epoxy resin.

SUPPORT FOR THE AMENDMENTS

Applicants have canceled Claims 1 and 2 and added new Claims 3-22. Support for new Claims 3, 11, and 19 can be found on page 10, line 4, to page 11, line 25, of the specification. Support for Claims 4, 12, and 20 can be found in Claim 2, as originally filed. Support for Claims 5 and 13 can be found on page 13, lines 2-11, of the specification. Support for Claims 6, 7, 14, 15, 21, and 22 can be found on page 10, lines 11-18, of the specification. Support for Claims 8 and 17 can be found on page 10, lines 4-11, of the specification. Support for Claims 9 and 18 can be found on page 10, lines 21-25, of the specification. Support for Claims 10 and 16 can be found on page 11, lines 10-14, of the specification.

No new matter has been added. Claims 3-22 are active in this application.

REMARKS

Present Claims 3-10 relate to a method for forming unevenness on the surface of an insulating layer, comprising:

(1) plasma etching a layer of an insulating resin composition, to obtain a plasma-treated insulating layer,

wherein said resin composition comprises a first resin and a second resin, and said first resin and said second resin have different plasma etching rates and said first resin and said second resin are not compatible with each other.

Present Claims 11-18 relate to a method for producing a multilayer printed-wiring board, comprising:

(1) plasma etching a layer of an insulating resin composition, to obtain a plasma-treated insulating layer; and

(2) forming a conducting layer on said plasma-treated insulating layer,

wherein said resin composition comprises a first resin and a second resin, and said first resin and said second resin have different plasma etching rates and said first resin and said second resin are not compatible with each other.

Present Claims 19-22 relate to multilayer printed-wiring boards prepared by such a method.

The inventors have discovered that the presently claimed methods of Claims 3-10 afford insulating layers with a roughened surface, which in turn afford superior bonding to a subsequently deposited conducting layer. Thus, the multilayer printed-wiring boards prepared by the methods of present Claims 11-18 and the multilayer printed-wiring boards of Claims 18-22 also exhibit the enhanced bonding between the insulating layer and the conducting layer.

The cited reference contains no disclosure which would suggest the presently claimed methods or multilayer printed-wiring boards. Accordingly, this reference cannot affect the patentability of the present claims.

The rejection of Claims 1 and 2 under 35 U.S.C. §103(a) in view of U.S. Patent No. 6,121,553 (Shinada et al) is respectfully traversed. Shinada et al disclose a resin composition including two kinds of resins which are not compatible with each other. However, Shinada et al is unconcerned with the use of plasma etching to roughen the surface of an insulating layer or the enhanced bonding between the insulating layer and a conducting layer afforded by such surface roughening of the insulating layer.

In contrast, the present claims all recite the step of "plasma etching" of the insulating layer. As described under the "Means to Solve the Problems" section bridging pages 6 and 7 of the present specification, the gist of the present invention lies in the facts:

The present inventors have conducted made extensive and intensive studies with a view to solving the above-mentioned problems. As a result, it has been found that the below-described resin composition has extremely excellent performance, on the basis of which the present invention has been completed.

Specifically, the present invention relates to an insulating resin composition for a multilayer printed-wiring board which composition is to be used to form, or as, an insulating layer of the multilayer printed-wiring board, wherein for obtaining a roughness or unevenness by plasma treatment on the surface of the insulating layer resulting from the insulating resin composition, the said insulating resin composition comprises two or more kinds of resins which are different in etching rate by a plasma treatment and which are not compatible with each other.

Thus, it has become possible to perform fine roughness formation treatment on the surface of the insulating layer by a dry treatment, such as a plasma treatment or the like. In this case, it is preferred that a surface roughness degree of the above-mentioned insulating layer by the plasma treatment is adjusted so as to be in the range of 100 to 4,000 nm.

Specification, pp. 6-7 (Emphasis added).

The benefits obtained by the presently claimed methods are described in the "Problems to be Solved by the Invention" section on page 6 of the present specification and the "Effect of the Invention" section bridging pages 25 and 26 thereof:

[Problems to be Solved by the Invention]

The present invention has been made for solving the above-mentioned problems effectively, and it is an object to provide an insulating resin composition for a multilayer printed-wiring board, which can ensure the bonding strength of a conductor layer with an insulating layer by performing a rough surface formation by a dry treatment, such as plasma or sputtering or the like, without performing a wet treatment which has conventionally been conducted for the rough surface formation, and can satisfy heat resistance and electrically insulating properties.

Specification, p. 6 (Emphasis added).

* * *

[Effect of the Invention]

As mentioned above, according to the insulating resin composition for a multilayer printed-wiring board of the present invention, the following excellent effects can be exhibited.

In the formation of the rough surface on the insulating layer for ensuring a satisfactory bonding force between the conductor layer and the insulating layer, not a wet treatment using an oxidant or the like which has been conventionally conducted but a dry treatment having high productivity, such as a plasma treatment or the like, can be employed. Thus, a stable form of a rough surface can be obtained without the conventional problems about cumbersome bath control and waste liquid treatment, and a high bonding strength can be realized. Further, by using this insulating resin composition, both of high heat resistance and excellent electrical properties can be achieved, and a multilayer printed-wiring board having a high wiring density can be produced.

Specification, pp. 25-26 (Emphasis added).

As compared with the presently claimed invention discussed above, Shinada et al indeed disclose use of a resin composition including two finds of resins which are not compatible with each other as an insulating layer. However, this reference does not disclose or suggest any roughening by a plasma treatment. In other words, the method of Shinada et al stops at a point where the resin composition is only used as an insulating layer, and does not go any further.

Accordingly, the rejection is no longer tenable and should be withdrawn.

Applicants acknowledge the Examiner's request in regard to Figure 2, and Applicants are complying therewith by filing herewith a request for approval of drawing change.

The objection to the specification has been obviated by appropriate amendment. As the Examiner will note, Applicants have amended page 5 of the specification such that it is

free of the criticism outline on page 2 of the Official Action. Accordingly, the objection is no longer tenable and should be withdrawn.

Applicants submit that the application is now in condition for allowance, and early notification of such action is earnestly solicited.

Respectfully submitted,

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